FIG. 1

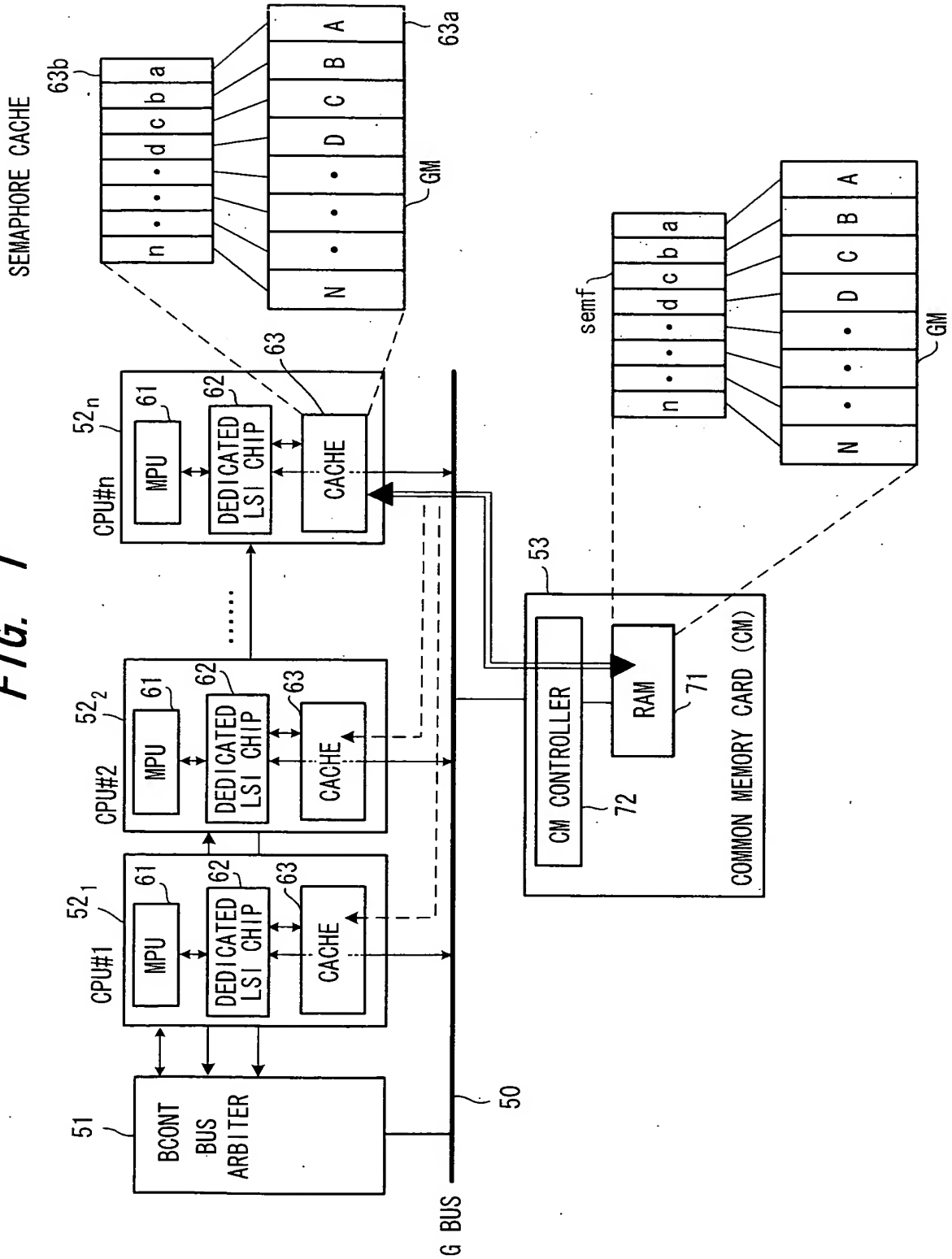
SEMAPHORE CACHE
63b
n • • d c b a
63a
N • • D C B A
GM
semf
n • • d c b a
N • • D C B A
GM
CPU#n
52n
MPU
61
DEDICATED LSI CHIP
62
CACHE
63
CPU#2
52 2
CPU#1
52 1
.....
51
BCONT BUS ARBITER
50
G BUS
53
CM CONTROLLER
72
RAM
71
COMMON MEMORY CARD (CM)

FIG. 2

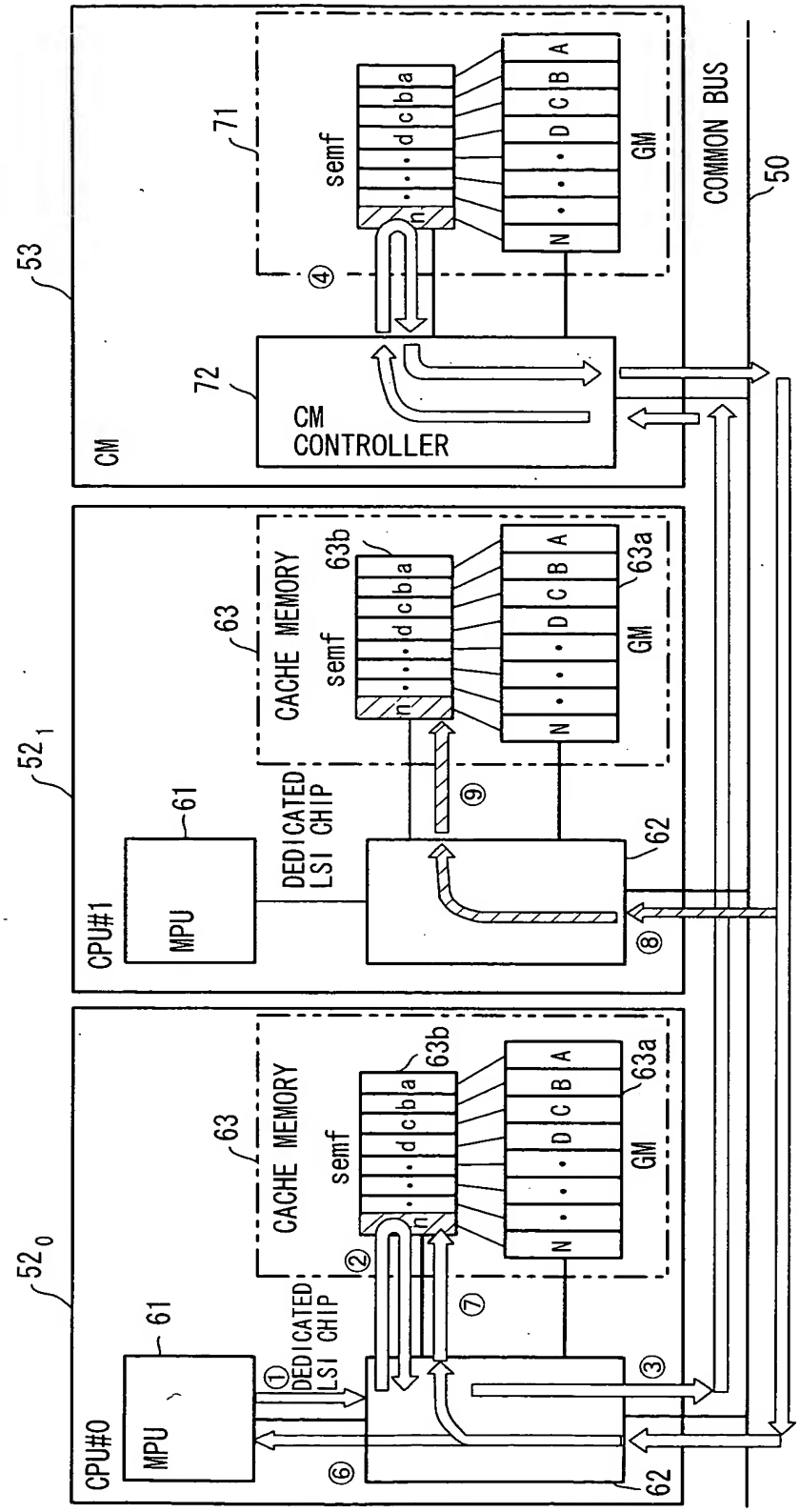
CM
CM CONTROLLER
72
71
semf
GM
COMMON BUS
50
53
CPU#1
MPU
61
DEDICATED LSI CHIP
CACHE MEMORY
63
63a
63b
62
CPU#0
52_0
52_1
①
②
③
④
⑤
⑥
⑦
⑧
⑨

FIG. 3

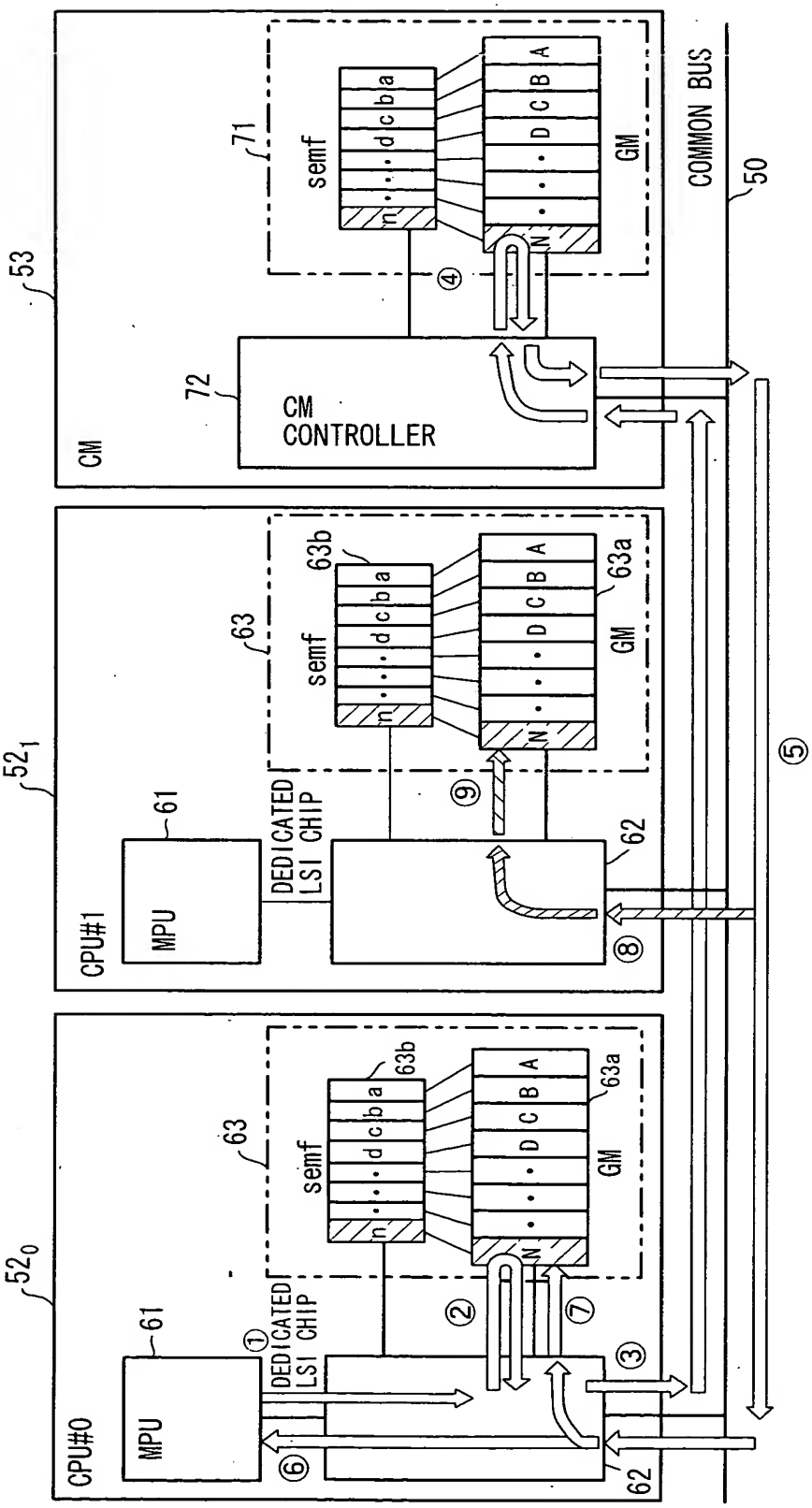
CM
CM CONTROLLER
72
53
71
semf
GM
COMMON BUS
50
CPU#1
MPU
61
DEDICATED LSI CHIP
63
63b
63a
62
CPU#0
52_1
52_0
①
②
③
④
⑤
⑥
⑦
⑧
⑨

FIG. 4

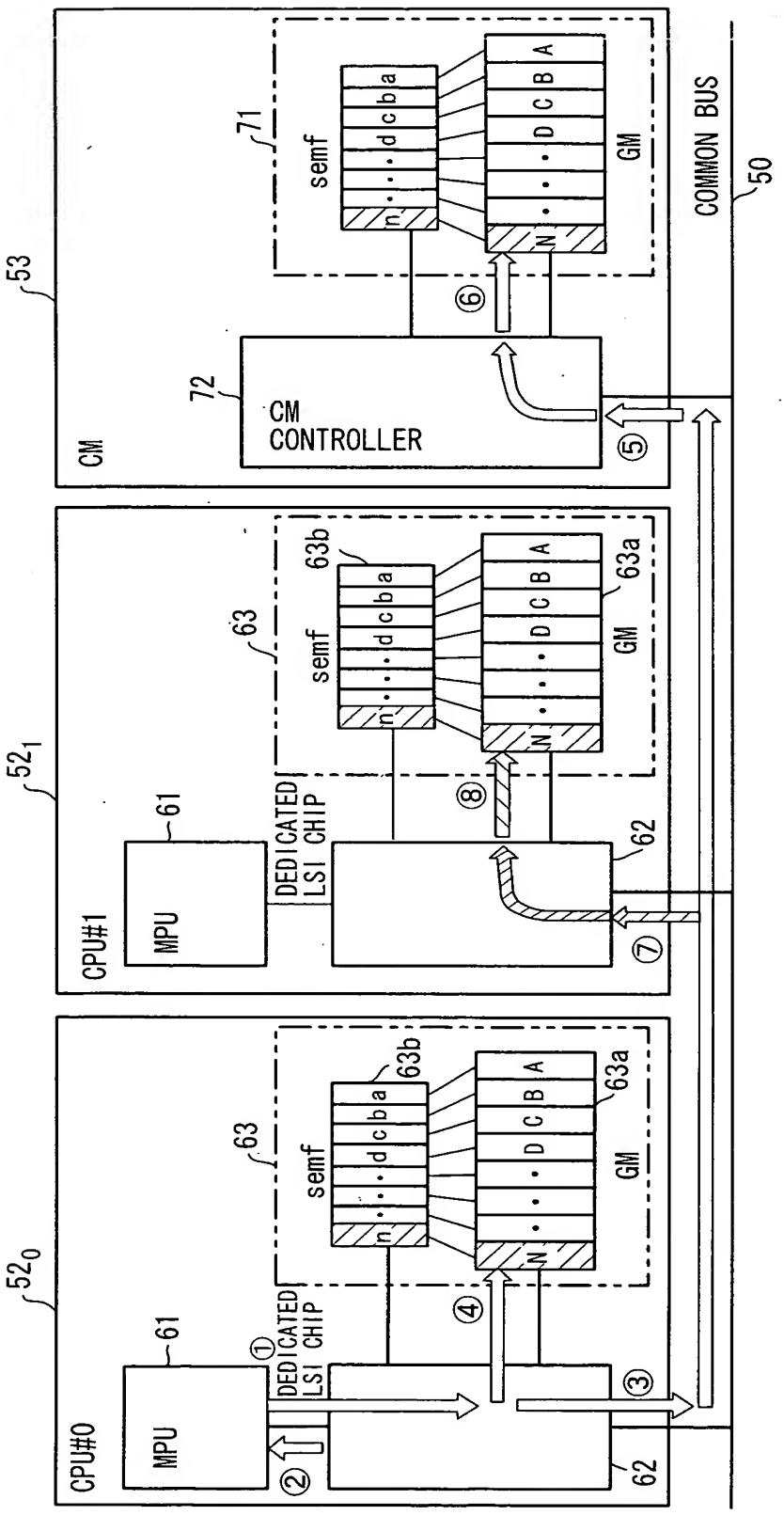
CPU#0
MPU
61
DEDICATED LSI CHIP
62
63
semf
63b
63a
GM
52₀
CPU#1
52₁
CM
CM CONTROLLER
72
71
53
COMMON BUS
50
①
②
③
④
⑤
⑥
⑦
⑧

FIG. 5

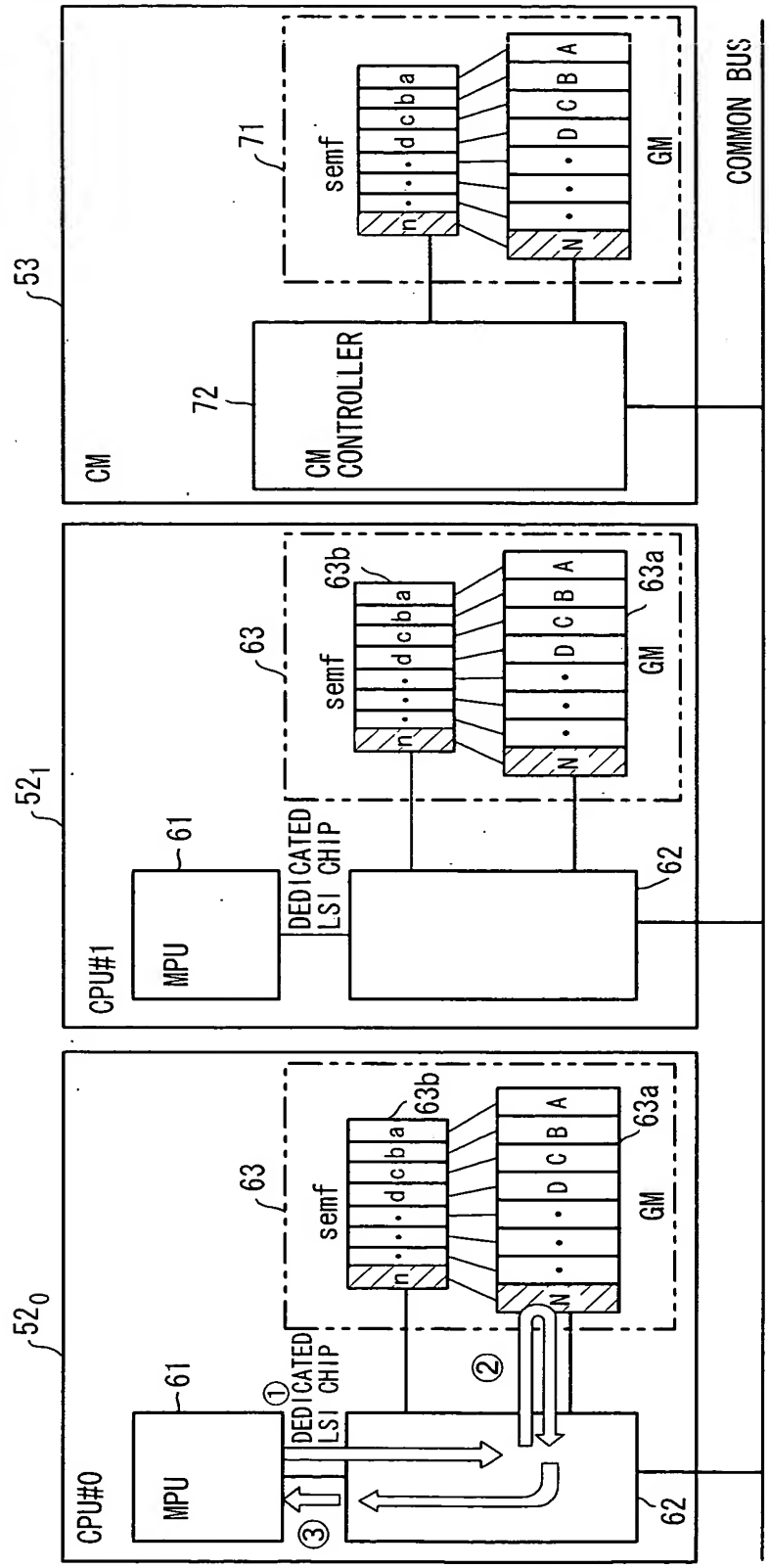
CPU#0
MPU
61
DEDICATED LSI CHIP
62
63
semf
63b
a b c d · · · n
63a
A B C D · · · N
GM
①
②
③
CPU#1
52_0
52_1
CM
CM CONTROLLER
72
71
53
COMMON BUS

FIG. 6

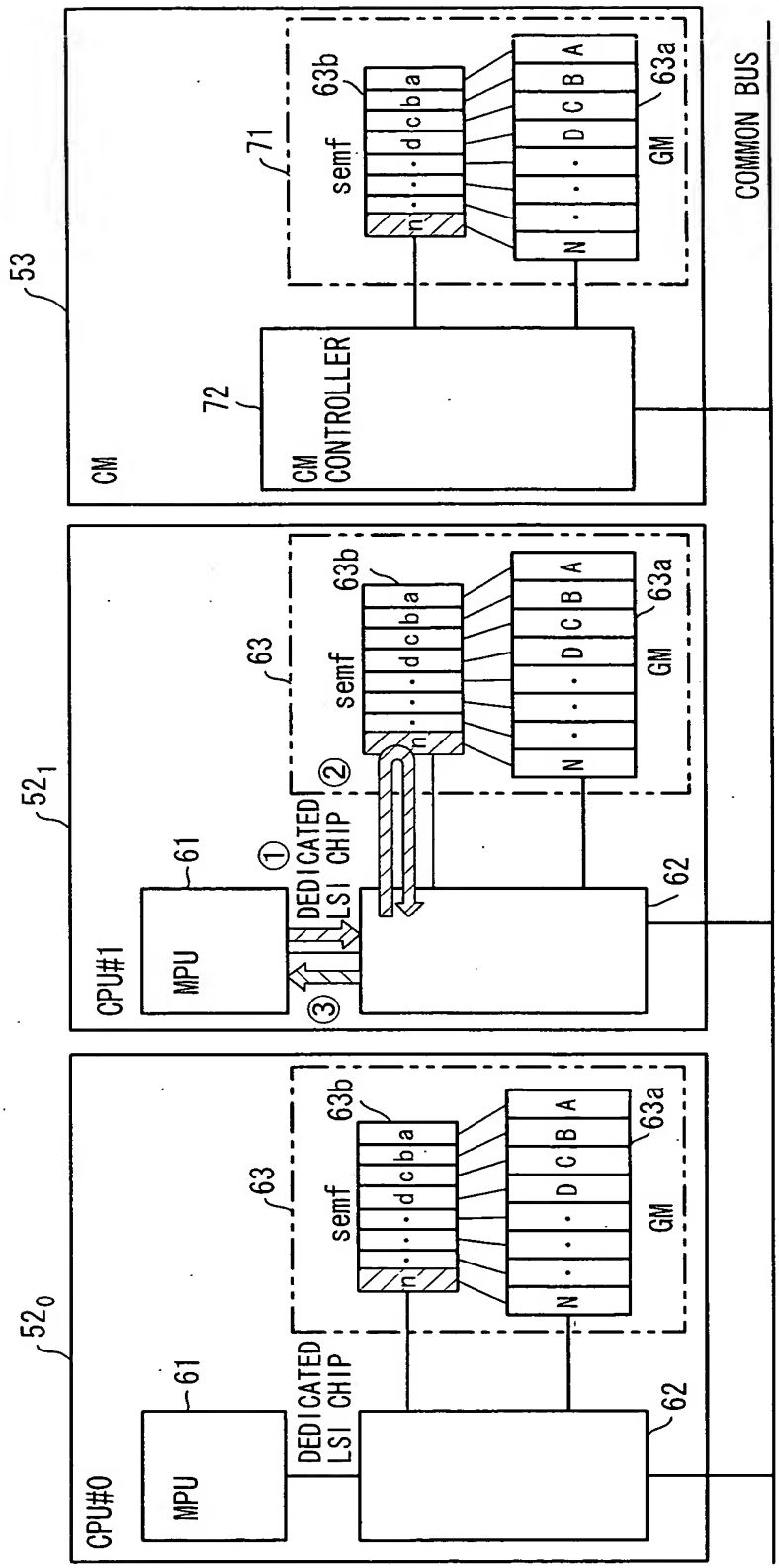
CPU#0
MPU
61
DEDICATED LSI CHIP
62
63
semf
63b
a b c d · · · n
63a
GM
A B C D · · · N
52₀
CPU#1
52₁
①
②
③
CM
53
CM CONTROLLER
72
71
COMMON BUS

FIG. 7

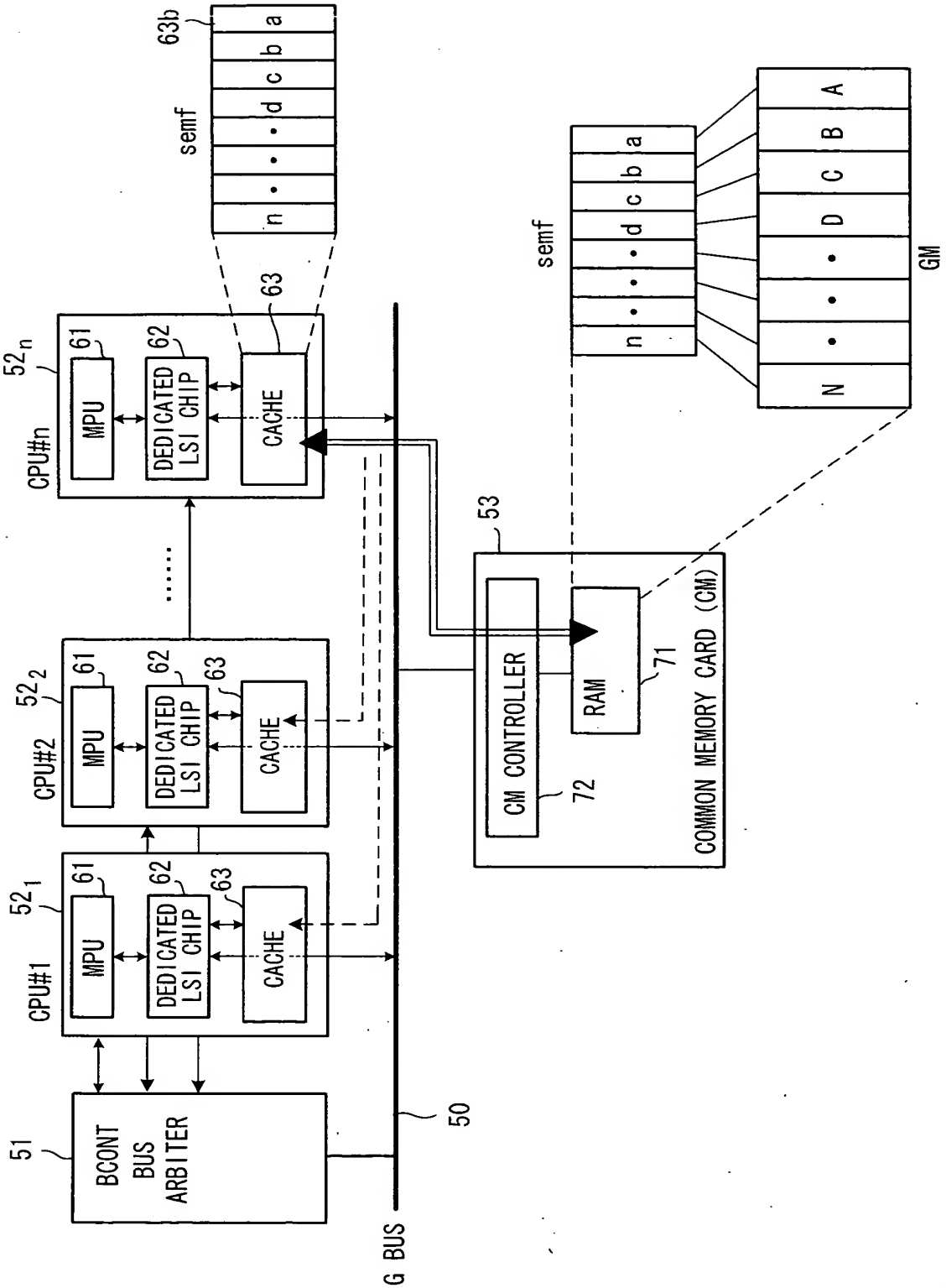
BCONT
BUS
ARBITER
51
50
G BUS
CPU#1
52 1
CPU#2
52 2
CPU#n
52 n
MPU
DEDICATED
LSI CHIP
CACHE
61
62
63
.....
53
CM CONTROLLER
72
RAM
71
COMMON MEMORY CARD (CM)
semf
n • • • d c b a
63b
semf
n • • • d c b a
N • • • D C B A
GM

FIG. 8

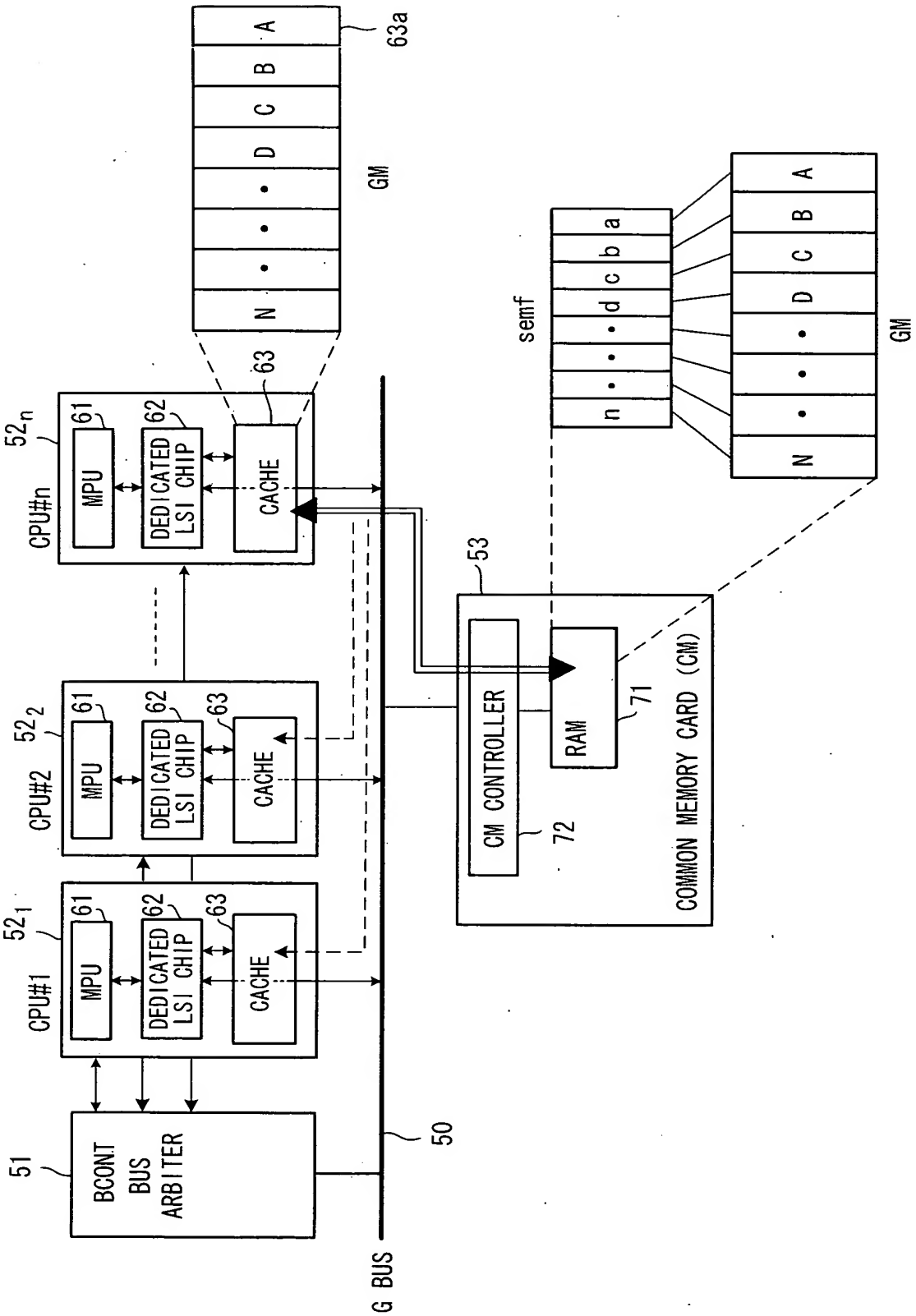
BCONT
BUS
ARBITER
51
50
G BUS
CPU#1
CPU#2
CPU#n
52 1
52 2
52 n
MPU
DEDICATED
LSI CHIP
CACHE
61
62
63
63a
GM
N • • • D C B A
n • • • d c b a
semf
CM CONTROLLER
72
RAM
71
53
COMMON MEMORY CARD (CM)

FIG. 9

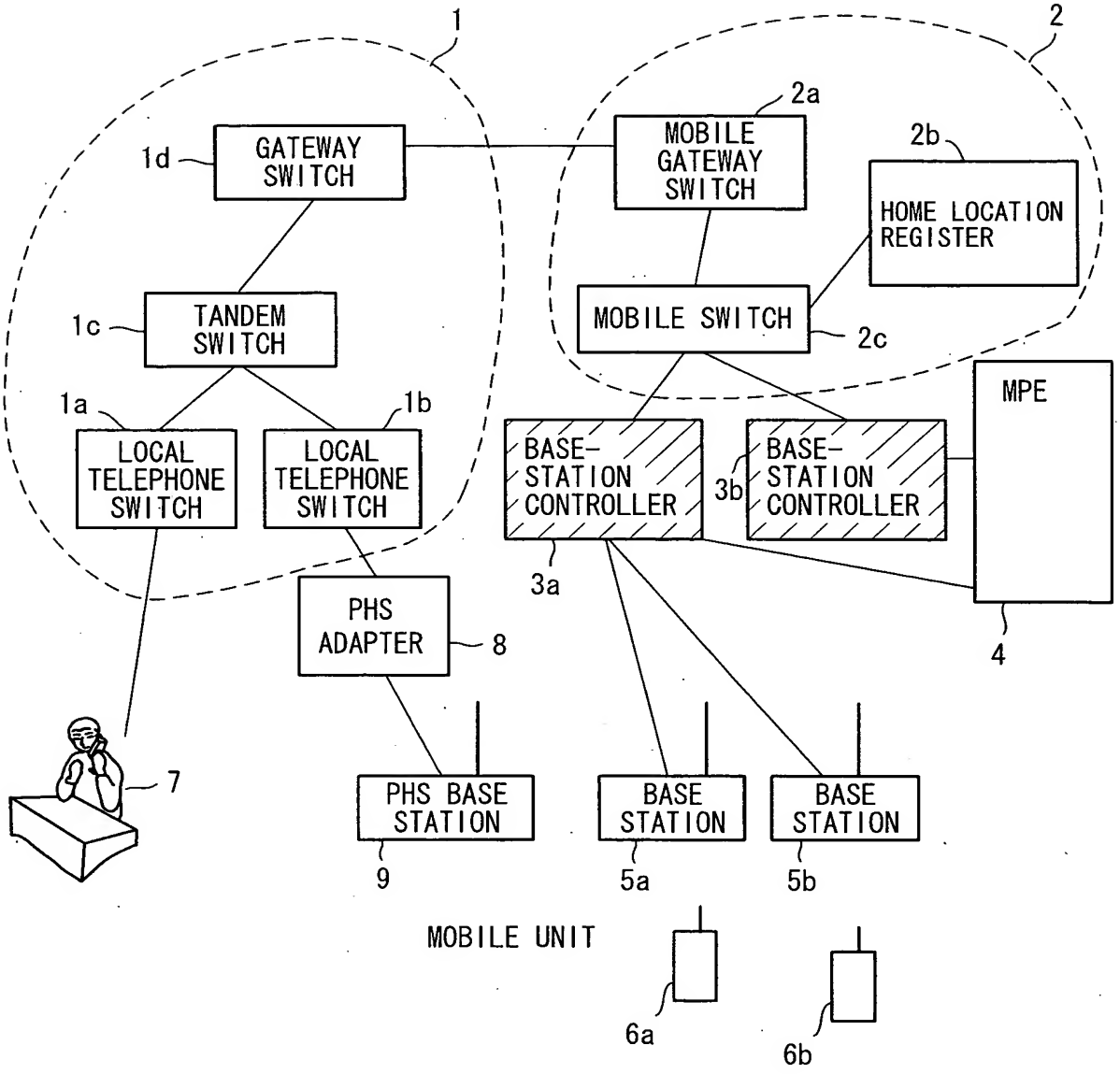
1
2
1d
GATEWAY SWITCH
2a
MOBILE GATEWAY SWITCH
2b
HOME LOCATION REGISTER
1c
TANDEM SWITCH
MOBILE SWITCH
2c
1a
1b
LOCAL TELEPHONE SWITCH
LOCAL TELEPHONE SWITCH
BASE-STATION CONTROLLER
3b
BASE-STATION CONTROLLER
MPE
3a
4
PHS ADAPTER
8
7
PHS BASE STATION
BASE STATION
BASE STATION
9
5a
5b
MOBILE UNIT
6a
6b

FIG. 10 PRIOR ART

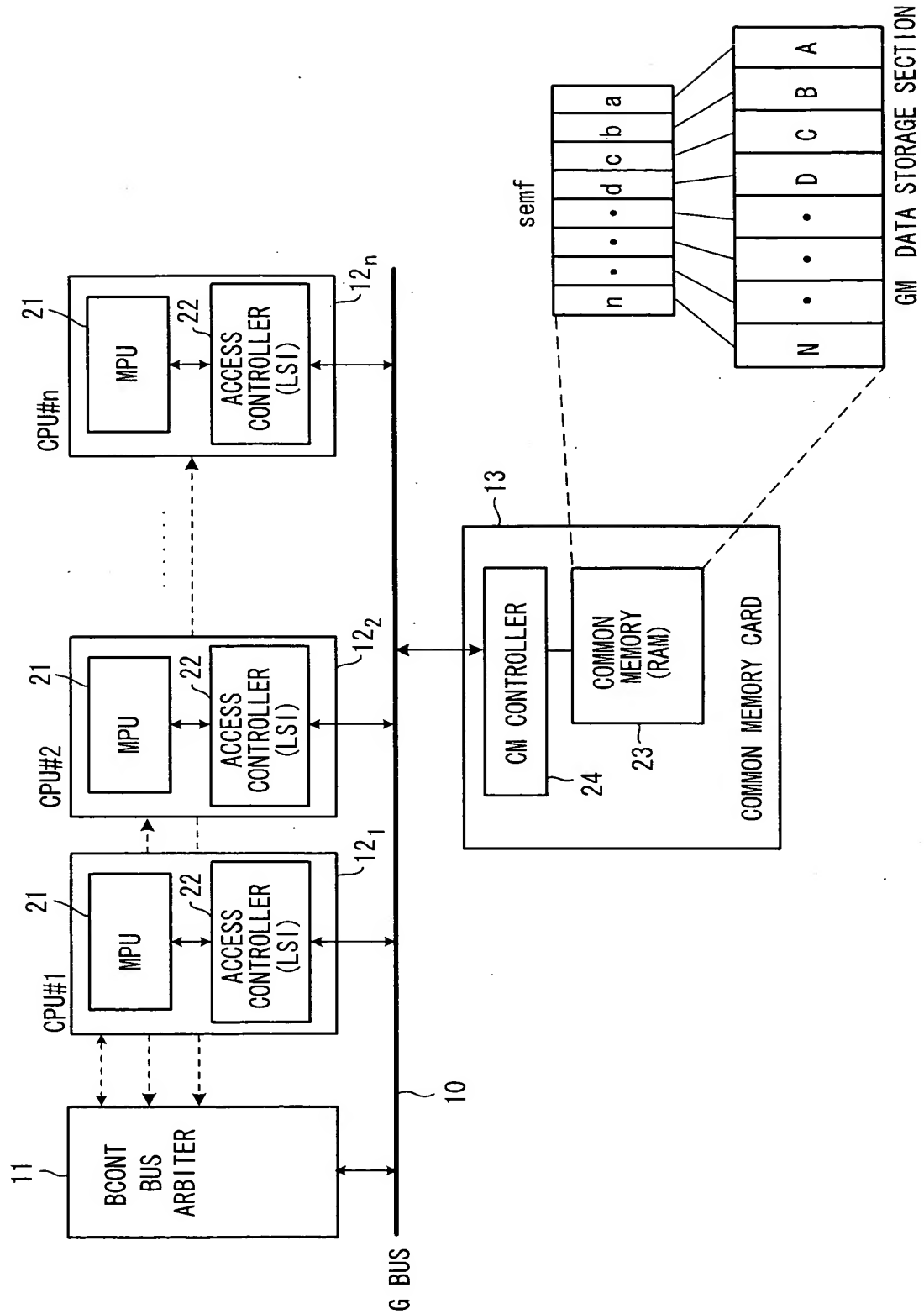

FIG. 11 PRIOR ART

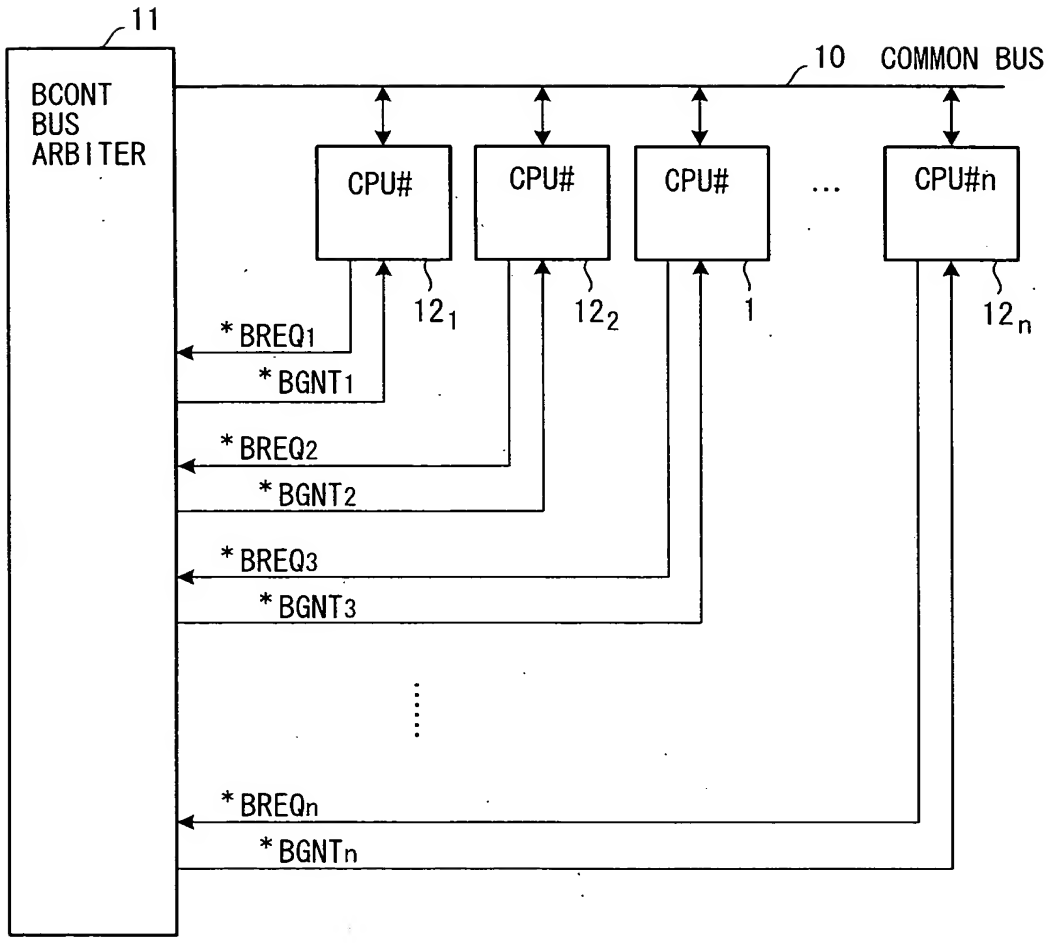

FIG. 12 PRIOR ART

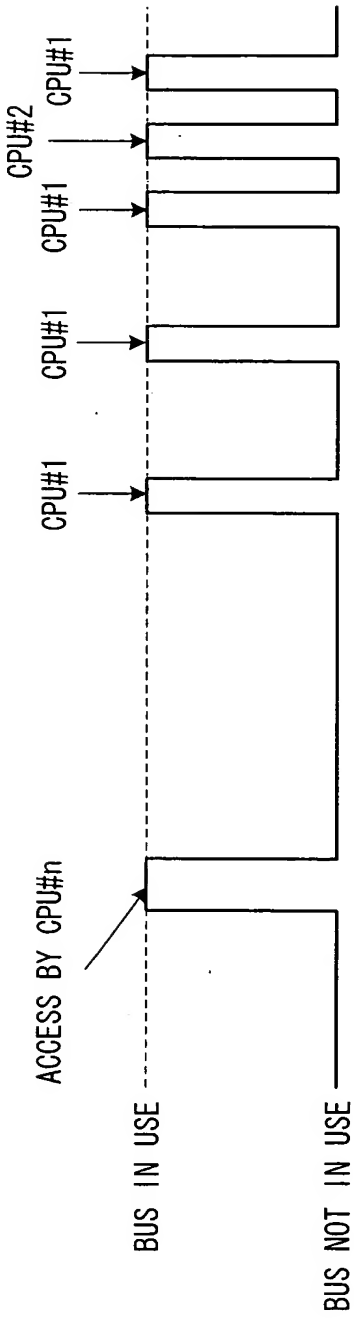

FIG. 13 PRIOR ART

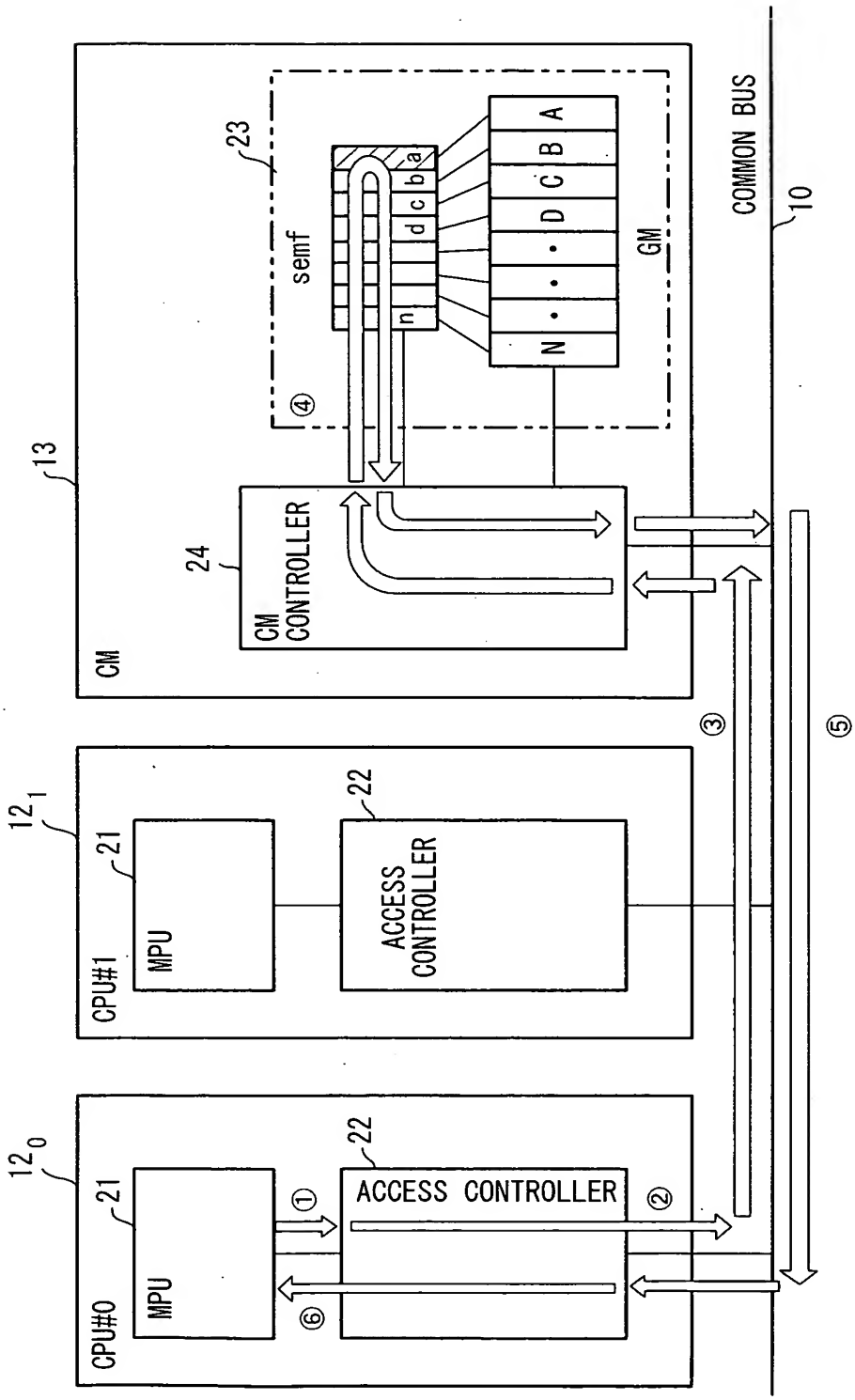

FIG. 14 PRIOR ART

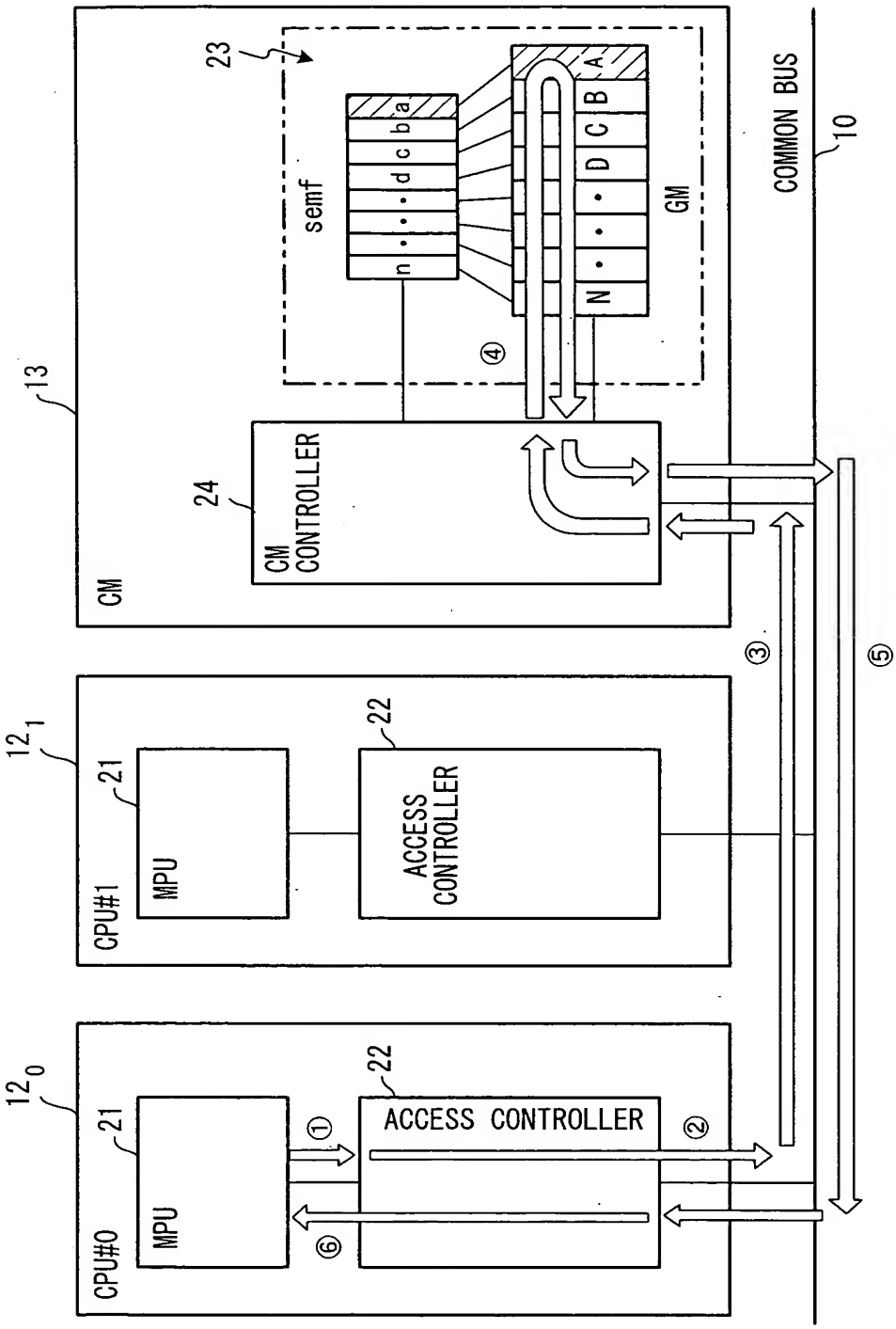

FIG. 15 PRIOR ART

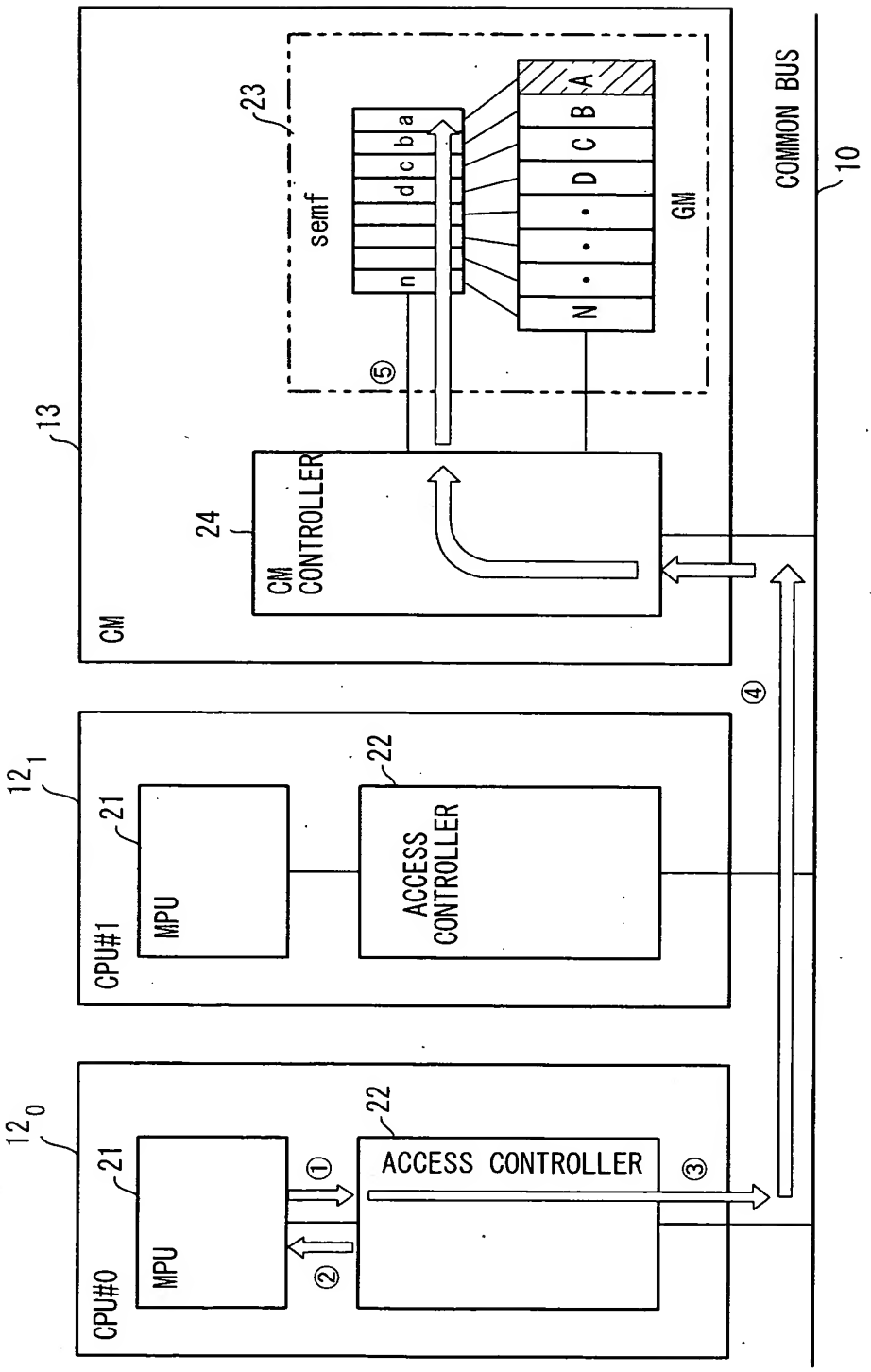

FIG. 16 PRIOR ART

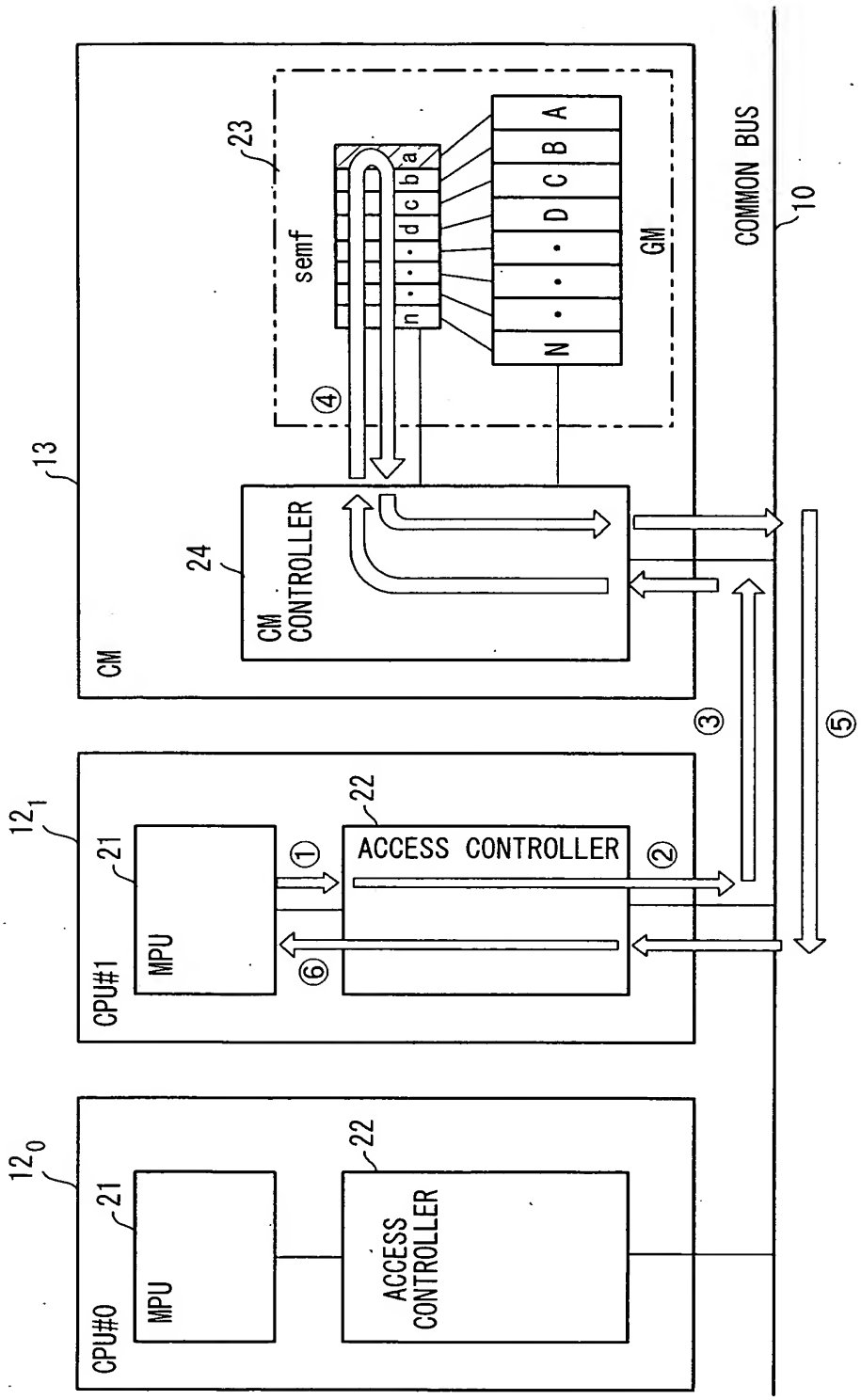

FIG. 17 PRIOR ART